We Claim:

1. A method for reading a memory cell in a semiconductor memory, which comprises:

providing a first bit line having a first portion connected to a memory cell and a second portion;

providing a second bit line having a first portion and a second portion, the first portion of the second bit line running opposite the first portion of the first bit line;

providing a sense amplifier having a first connection and a second connection carrying a complementary signal with respect to the first connection of the sense amplifier;

providing a first switch for connecting the first portion of the first bit line to the first connection of the sense amplifier;

providing a second switch for connecting the first portion of the second bit line to the second connection of the sense amplifier;

providing a third switch for connecting the second portion of the first bit line to the first connection of the sense amplifier;

providing a fourth switch for connecting the second portion of the second bit line to the second connection of the sense amplifier;

providing a first precharging circuit connected to the first portion of the first bit line and connected to the first portion of the second bit line;

providing a second precharging circuit connected to the second portion of the first bit line and connected to the second portion of the second bit line;

in a first phase, controlling the first switch, the second switch, the third switch, and the fourth switch to be conductive;

in a subsequent second phase, controlling the third switch to be blocked while the first switch, the second switch and the fourth switch are conductive and the memory cell is coupled to the first portion of the first bit line for reading a stored data value;

in a subsequent third phase, controlling the third switch and the fourth switch to be blocked while the first switch and the

second switch are conductive and the sense amplifier is enabled for amplification; and

in a subsequent fourth phase, controlling the first switch, the second switch, the third switch and the fourth switch to be conductive.

2. The method according to claim 1, which further comprises controlling the first precharging circuit to be on during the first phase and controlling the first precharging circuit to be off during the second phase and the third phase.

3. The method according to claim 1, which further comprises controlling the second precharging circuit to be on during the first phase, the second phase, and the third phase.

4. The method according to claim 1, which further comprises controlling the second precharging circuit to be on during the first phase and controlling the second precharging circuit to be off during the second phase and the third phase.

5. A semiconductor memory, comprising:

at least one memory cell;

a first bit line having a first portion connected to said memory cell and a second portion;

a second bit line having a first portion and a second portion, said first portion of said second bit line running opposite said first portion of said first bit line;

a sense amplifier having a first connection for carrying a signal and a second connection for carrying a complementary signal with respect to said signal on said first connection of said sense amplifier;

a first switch for connecting said first portion of said first bit line to said first connection of said sense amplifier;

a second switch for connecting said first portion of said second bit line to said second connection of said sense amplifier;

a third switch for connecting said second portion of said first bit line to said first connection of said sense amplifier;

a fourth switch for connecting said second portion of said second bit line to said second connection of said sense amplifier;

a first precharging circuit connected to said first portion of said first bit line and connected to said first portion of said second bit line;

a second precharging circuit connected to said second portion of said first bit line and connected to said second portion of said second bit line; and

a control circuit for controlling said first switch, said second switch, said third switch, and fourth switch, said first precharging circuit, and said second precharging circuit such that:

in a first phase, said first switch, said second switch, said third switch, and said fourth switch are conductive;

in a subsequent second phase, said third switch is blocked while said first switch, said second switch and said fourth switch are conductive, and said memory cell is connected to said first portion of said first bit line for reading a data value stored in said memory cell;

in a subsequent third phase, said third switch and said fourth switch are blocked while said first switch and

said second switch are conductive and said sense amplifier is enabled for amplification; and

in a subsequent fourth phase, said first switch, said second switch, said third switch and said fourth switch are conductive.